17.5 A 1.2mW 0.02mm² 2GHz Current-Controlled PLL Based on a Self-Biased Voltage-to-Current Converter

WooYoung Jung, HyoungChul Choi, ChangWon Jeong, KwiYoung Kim, WooSeok Kim, HaJun Jeon, GyeSoo Koo, JiHyun Kim, JinHo Seo, MyeongLyong Ko, JaeWhui Kim

Samsung Electronics, Yongin, Korea

Phase-locked loops (PLLs) are widely used for generating the different clocks required in ASIC and SoC designs. In order to cover the various clock frequencies with a single PLL, the PLL has to provide a wide range of frequencies while keeping optimal bandwidth and jitter performance. The bandwidth of a PLL should be independent of the multiplication factor as well as process, voltage and temperature (PVT).

Furthermore, small size and low power consumption are required. This work proposes a novel approach to achieve a constant bandwidth with respect to the multiplication factor and PVT variations. A simple current-controlled method based on a self-biased voltage-to-current (V-I) converter makes the PLL bandwidth depend only on the reference frequency and allows a small loop filter to be used.

In conventional PLL designs, the output frequency and bandwidth are inherently related to the multiplication factor. Other approaches have been tried to solve this problem: In [3], a multistage inverse-linear programmable current mirror was used to make the bandwidth independent of the multiplication factor while sacrificing area and power because of the 12b current DAC. In [4], a PLL with a current-mode filter is proposed to make bandwidth independent of PVT variations and multiplication factor. It adopts a noise-canceling circuit and a regulated cascode current source because of the switch noise and low power-supply noise rejection ratio (PSRR) in the current-mode filter [4,5]. The correlation coefficient is defined to be 1 (low I_{CCO} frequency) and 1/2 (high I_{CCO} frequency) without explanation [4].

The PLL architecture presented here uses the current-controlled method based on a self-biased V-I converter as shown in Fig. 17.5.1(a). The charge pump current (I_{CP}) and the current-controlled oscillator current (I_{CCO}) are proportional to the V-I converter current (I_X). The resistor (R) of the converter controls the overall ranges of the currents.

The combined PLL's linear model gives a closed-loop transfer function of

$$G(s)=\frac{\phi_{OUT}}{\phi_{REF}}=\frac{\frac{I_{CP}}{2\pi}\cdot H(s)\cdot\frac{1}{R}\cdot\frac{I_{CCO}}{I_X}\cdot\frac{K_{CCO}}{s}}{1+\frac{I_{CP}}{2\pi}\cdot H(s)\cdot\frac{1}{R}\cdot\frac{I_{CCO}}{I_X}\cdot\frac{K_{CCO}}{s}\cdot\frac{1}{M}} \quad (1)$$

where K_{CCO} is the gain of the current-controlled oscillator and $H(s)$ is the transfer function of the loop filter.

The gain of the current-controlled oscillator (K_{CCO}) can be written as:

$$K_{CCO}=\frac{F_{OUT}-K}{I_{CCO}} \quad (2)$$

where K is the intercept to the frequency axis of the CCO gain curve (f-I curve) in Hz.

The PLL bandwidth can be approximated as a second-order system with

$$\omega_B=\eta\cdot\frac{I_{CP}}{I_X}\cdot\frac{R_{LP}}{R}\cdot F_{REF} \quad (3)$$

where R_{LP} is the resistor of the second-order loop filter.

Equation (3) indicates that the PLL bandwidth is determined by F_{REF}, η (η = 0.7) and the ratios of currents and resistors. The correlation coefficient η depends on the linearity of the CCO gain (related to K) and the operating frequency. The PLL bandwidth is independent of PVT variations and even the multiplication factor (M), without requiring any additional circuitry as in previous works [1,3,4].

A detailed schematic of the current-controlled method based on a self-biased V-I converter is shown in Fig. 17.5.1(b). In order to reduce the power consumption, the 1.0V logic power supply is used instead of introducing a second power supply for the PLL. The self-biased V-I converter is designed as a master control block and provides currents to the sub-blocks in proportion to the size of the current mirror. To improve the dynamic PSRR for the supply noise in the 1.0V supply voltage, this work uses the following approaches: 1) the currents of the charge pump, the CCO and the differential-to-single-ended converter (DTS) are regulated by the V-I converter. 2) A decoupling capacitor is placed between the inverter chain and the power. 3) NMOS and PMOS transistors with 1µm lengths are used for current bias. 4) High loop bandwidth (F_{REF}/10) is chosen to reduce low-frequency power supply noise.

Figure 17.5.2 shows the current-controlled oscillator (CCO) circuit, which consists of four stages of pseudo-differential CMOS inverters. It achieves high PSRR, low power operation and linear gain in a wide operating frequency range [2,5]. The proposed DTS is also illustrated in Fig. 17.5.2. The pre-amplifier and the full-swing amplifier are used to obtain a high gain and a wide bandwidth. The clock buffer drives the load with a 50% duty-cycle rail-to-rail output. To attain the differential rail-to-rail outputs, a clock buffer is added to the other output in the full-swing amplifier. The proposed DTS provides low power consumption with a wide range of operating frequencies by eliminating the short-circuit current in the pre-amplifier and the full-swing amplifier. The gain curve and the duty-cycle of the CCO, and the power consumptions of both the CCO and DTS are shown in Fig. 17.5.3. The CCO with the DTS has a duty-cycle of 50% ±1% over the CCO frequency range and the DTS draws less than 150µA at 2GHz including the clock buffers.

Figure 17.5.4 shows the calculated values and their regression lines for K and η. K can be obtained from the gain curve of the CCO (f-I curve) in Fig. 17.5.3. η has a value between 0.6 (at high frequency) and 0.8 (at low frequency) because of the K_{CCO} variation (K variation). The calculated and the measured bandwidths are plotted as functions of the multiplication factor (M) and F_{REF} in Fig. 17.5.4. The bandwidth is almost independent of the multiplication factor (M) and directly proportional to F_{REF} as expected.

The 1.0V current-controlled PLL in this paper has been implemented in a 90nm 1P4M CMOS process. It consumes 1.2mW at a 2GHz operating frequency with 1.0V power supply. The PLL is designed for a bandwidth of 400kHz at 4MHz F_{REF} with a second-order loop filter. The PLL bandwidth will track one-tenth of F_{REF}. The PLL includes a 10b dual-modulus programmable main divider, a 6b programmable pre-divider and a 3b post-divider. The frequency range is from 500MHz to 2GHz in mass production. The die area is 141µm×142µm as shown in Fig. 17.5.7. The jitter of the PLL operating at 1GHz is shown in Fig. 17.5.5. The RMS and peak-to-peak jitters at 1GHz are 5.69ps and 38ps respectively, while consuming 0.7mW. The overall PLL performance is summarized in Fig. 17.5.6.

References:

[1] J. G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, pp. 1723-1732, Nov., 1996.

[2] K. Y. Chang et al., "A 0.4-4Gb/s CMOS Quad Transceiver Cell using On-chip Regulated Dual-Loop PLLs," *Symp. VLSI Circuits*, pp. 88-91, Jun., 2002.

[3] J. G. Maneatis et al., "Self-Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL," *IEEE J. Solid-State Circuits*, pp. 1795-1803, Nov., 2003.

[4] Gang Yan et al., "A Self-Biased PLL with Current-Mode Filter for Clock Generation," *ISSCC Dig. Tech. Papers*, pp. 420-421, 2005.

[5] M. Mansuri and C.-K.K. Yang, "A Low-Power Adaptive Bandwidth PLL and Clock Buffer with Supply-Noise Compensation," *IEEE J. Solid-State Circuits*, pp. 1804-1812, Nov., 2003.

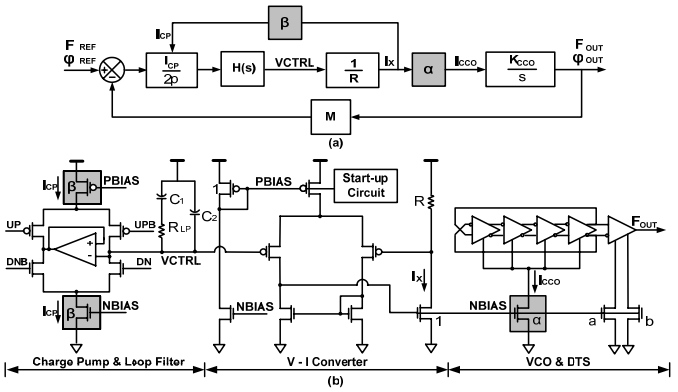

Figure 17.5.1: The block diagram (a), and the complete schematic of the current-controlled PLL with self bias technique (b).

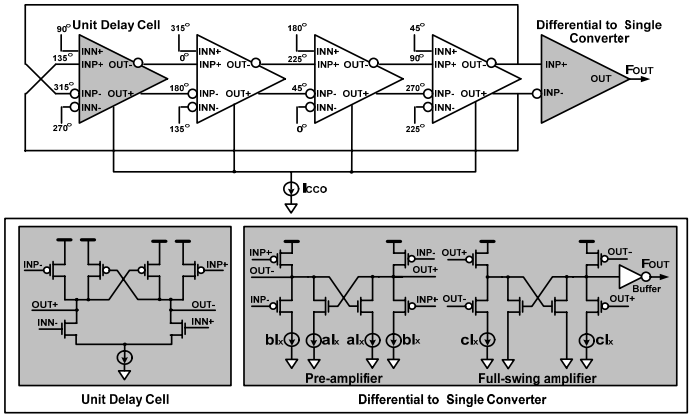

Figure 17.5.2: Quadrature pseudo-differential current-controlled oscillator and the differential-to-single-ended converter.

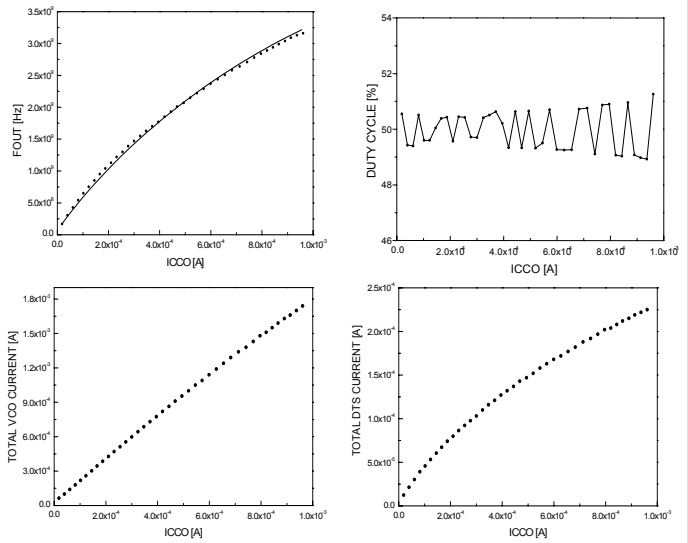

Figure 17.5.3: VCO curve, Duty Cycle and Currents for the CCO and DTS.

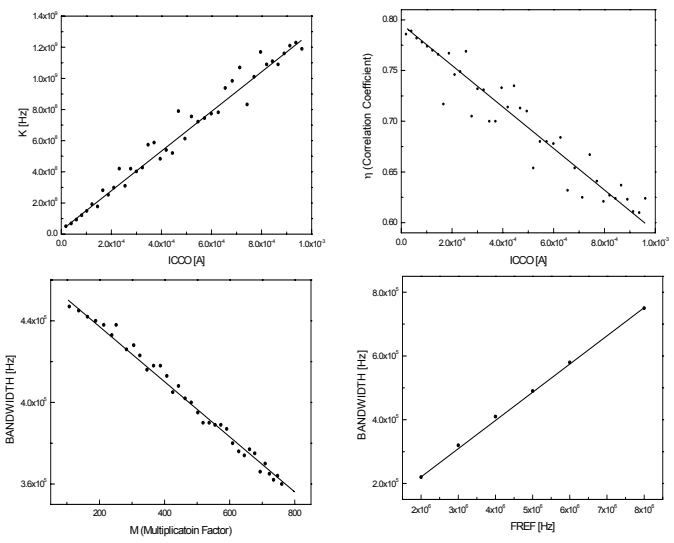

Figure 17.5.4: *K*, *η*, and Bandwidth as functions of *M* and F_{REF}.

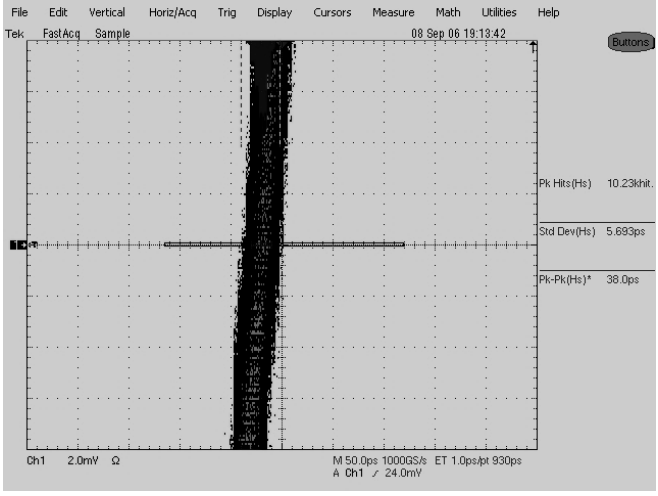

Figure 17.5.5: Jitter of the PLL @ 1GHz.

Process	90nm 1 poly 4 metal CMOS
Supply Voltage	1.0V
Frequency Range	0.5 to 2GHz
Input Frequency Range (FREF)	2 to 8MHz
Bandwidth	200 to 800KHz (F_{REF}/10)
Loop Filter	R_{LP} (36.2KΩ), C_{MAIN}(44pF), C_{RIPPLE}(2.7pF)
Period Jitter	5.8ps (rms), 34ps (peak-peak)@1GHz
Power Dissipation	1.2mW @2GHz (0.7mW@1GHz)
Active Die Area	0.02mm² (=141μm × 142μm)

Figure 17.5.6: Performance summary for the PLL.

Continued on Page 605

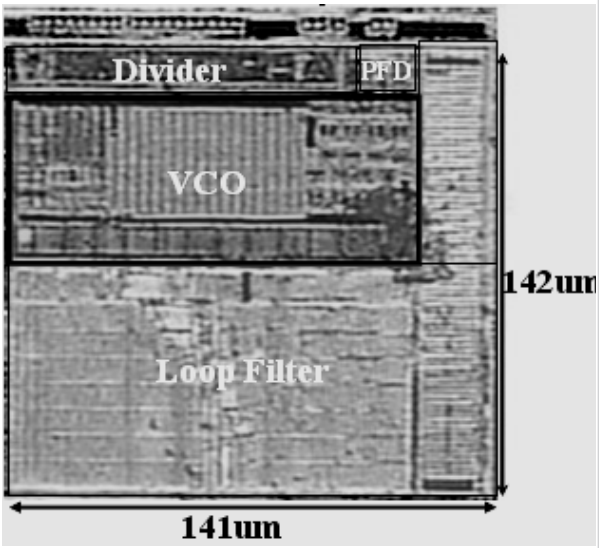

Figure 17.5.7: Die micrograph of the PLL.

